REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 3-6, 8-11, and 13-20 are pending in this case. Claims 2, 7, and 12 have been canceled without prejudice or disclaimer. Claims 1-3-6, 8-12, and 13-16 are amended by the present amendment to include the subject matter of the canceled claims without the introduction of any new matter.

The outstanding Official Action includes a rejection of Claims 1-3, 6-8, 11-13, and 16-20 under 35 U.S.C. §103(a) as being unpatentable over Kan (U.S. Patent No. 5,355,508) in view of Venable (U.S. Patent No. 6,705,456), a rejection of Claims 4, 9, and 14 under 35 U.S.C. §103(a) as unpatentable over Kan in view of Venable in further view of Arimilli et al. (U.S. Patent No. 6,023, 746, Arimilli), a rejection of Claims 5, 10, and 15 under 35 U.S.C. §103(a) as unpatentable over Kan in view of Venable in further view of Yamagami et al. (U.S. Patent No. 6,229,954, Yamagami).

The rejection of Claims 1-3, 6-8, 11-13, and 16-20 under 35 U.S.C. §103(a) as being unpatentable over Kan in view of Venable is traversed because each of these claims include the require selection of a transfer mode from an existing plurality of transfer modes. Note, for example, the requirement of Claim 1 that there must be:

> a memory controller section configured to be responsive to the control register section outputs to control selection of one data transfer mode from a plurality of data transfer modes available to provide different data transfer operations between the arithmetic processing unit and the memory, said transfer modes including at least a random access transfer mode in which a memory address must be included to access the memory for said data transfer and at least one other data transfer mode.

It is clear that there is nothing disclosed or suggested by Kan and/or Venable that meets such claim requirements.

The outstanding Action has pointed to Kan at col. 6, lines 34-42 as some how teaching the previous recitals of canceled Claim 2 as to transfer mode selection. However, the present claim language requires selection of "one data transfer mode from a plurality of data transfer modes available to provide different data transfer operations between the arithmetic processing unit and the memory, said transfer modes including at least a random access transfer mode in which a memory address must be included to access the memory for said data transfer and at least one other data transfer mode." The teachings at col. 6, lines 34-42 are merely that data is transferred between the memory and the arithmetic processing unit,[1] not that plural modes are available for selection and that one of these transfer modes is actually selected.

Claim 3 and Claims 17-20 are dependent from independent Claim 1, Thus, Claims 3 and 17-20 are also believed to be patentable for these reasons as well as for the reason that the added subject matter thereof is not taught or suggested by Kan and/or Venable taken alone or together in any proper combination.

Applicants respectfully traverse the further rejection of Claims 6, 8, 11, 13, and 16 under 35 U.S.C. §103(a) as unpatentable over Kan in view of Venable. In this regard, Claim 6 is an independent "means" claim with comparable limitations to those of Claim 1. Similarly, Claim 11 is a method claim reciting steps comparable to the limitations of Claim 1. Accordingly, Claims 6 and 11 are considered to patentably define over Kan in view of Venableer for the above noted reasons presented as to Claim 1 subject matter.

As Claim 8 depend on Claim 6 and as Claim13 depend on Claim 11, these dependent claims are believed to patentably define over Kan in view of Venableer for the above noted reasons as well.

---

[1] Col. 6, lines 34-42 state "[t]he control of the whole SIMD type parallel data processing unit 50 is performed by the system controller 11, from which the same instructions are issued to all the processing elements 108 at the same time. Data to be processed are transmitted from the common memory 42 to each of the processing elements 108 through the input controller 103 in response to instructions from the system controller 11. In addition, processed data are returned to the common memory 42 through the output controller 102."

Applicants further respectfully traverse the rejection of dependent Claims 8, and 13 under 35 U.S.C. §103(a) as unpatentable over Kan in view of Venable because these dependent Claims 8 and 13 recite additional features not taught or suggested by the applied references.

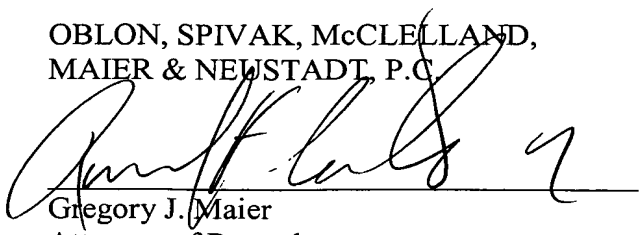
Applicants respectfully traverse the rejection Claims 4, 9, and 14 under 35 U.S.C. §103(a) as unpatentable over Kan in view of Venable in further view of Arimilli and the rejection of Claims 5, 10, and 15 under 35 U.S.C. §103(a) as unpatentable over Kan in view of Venable in further view of Yamagami. In this regard, neither Arimilli nor Yamagami cures the above noted deficiencies of the primary combination of Kan and Venable.

Applicants further respectfully traverse the rejection of Claims 4, 9, and 14 under 35 U.S.C. §103(a) as unpatentable over Kan in view of Venable in further view of Arimilli and the rejection of Claims 5, 10 and 15 under 35 U.S.C. §103(a) as unpatentable over Harrell in view of Venable and further in view of Yamagami because Claims 4, 5, 9, 10, 14, and 15 recite additional features not taught or suggested by the applied references.

Accordingly, the outstanding rejections are traversed and the pending claims are believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Attorney of Record
Registration No. 25,599

Raymond F. Cardillo, Jr.
Registration No. 40,440

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)

I:\ATTY\ET\201392US\201392US-AMD1.DOC